实验三实验结论  
  
1. Protues电路图

（1）全加器电路（截图）  
  
（2）四位加/减可控运算电路（截图）  
  
2. Protues仿真效果图（全加器、四位加/减可控运算电路）  
  
（1）全加器电路（截图）  
  
（2）四位加/减可控运算电路（截图）  
  
3.Quartus顶层文件（一位全加器、四位全加器、四位减法器）  
  
（1）全加器电路  
module logic3\_a(ain,bin,cin,cout,sum);  
  
inputain,bin,cin;  
  
outputcout,sum;  
  
assign{cout,sum} = ain+bin+cin;  
  
endmodule  
（2）四位全加器  
module logic3\_b(ain,bin,cin,cout,sum);

input[3:0] ain,bin;

input cin;

output cout;

output[3:0]sum;

assign{cout,sum} = ain+bin+cin;

endmodule

（3）四位减法器  
module sub\_4bits(ain,bin,cin,cout,sum);

input[3:0] ain,bin;

input cin;

output cout;

output[3:0]sum;

assign{cout,sum} = ain-bin-cin;

endmodule  
4.Quartus测试文件（一位全加器、四位全加器、四位减法器）  
  
（1）全加器电路（完整测试文件）  
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// This file contains a Verilog test bench template that is freely editable to

// suit user's needs .Comments are provided in each section to help the user

// fill out necessary details.

// \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

// Generated on "03/08/2020 11:38:59"

// Verilog Test Bench template for design : logic3\_a

//

// Simulation tool : ModelSim-Altera (Verilog)

//

`timescale 1 ns/ 1 ps

module logic3\_a\_vlg\_tst();

// constants

// general purpose registers

reg eachvec;

// test vector input registers

reg ain;

reg bin;

reg cin;

// wires

wire cout;

wire sum;

// assign statements (if any)

logic3\_a i1 (

// port map - connection between master ports and signals/registers

.ain(ain),

.bin(bin),

.cin(cin),

.cout(cout),

.sum(sum)

);

initial

begin

// code that executes only once

// insert code here --> begin

ain=0;

bin=0;

cin=0;

#20

bin=1;

cin=1;

#10

ain=1;

#30

bin=0;

cin=0;

#40

ain=0;

cin=1;

#10

ain=0;

bin=0;

cin=0;

#20

$finish;

// --> end

$display("Running testbench");

end

endmodule  
（2）四位全加器（完整测试文件）  
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// Generated on "03/13/2020 20:48:35"

// Verilog Test Bench template for design : logic3\_b

//

// Simulation tool : ModelSim-Altera (Verilog)

//

`timescale 100 ns/ 1 ps

module logic3\_b\_vlg\_tst();

// constants

// general purpose registers

//reg eachvec;

// test vector input registers

reg [3:0] ain;

reg [3:0] bin;

reg cin;

// wires

wire cout;

wire [3:0] sum;

// assign statements (if any)

logic3\_b i1 (

// port map - connection between master ports and signals/registers

.ain(ain),

.bin(bin),

.cin(cin),

.cout(cout),

.sum(sum)

);

initial

begin

// code that executes only once

// insert code here --> begin

ain=0;

bin=0;

cin=0;

#20

ain=6;

cin=1;

#30

bin=11;

cin=0;

#40

ain=1;

bin=2;

#50

bin=15;

cin=1;

#10

$finish;

// --> end

$display("Running testbench");

end

endmodule

（3）四位减法器（完整测试文件）

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// Generated on "03/13/2020 21:42:06"

// Verilog Test Bench template for design : sub\_4bits

//

// Simulation tool : ModelSim-Altera (Verilog)

//

`timescale 100 ns/ 1 ps

module sub\_4bits\_vlg\_tst();

// constants

// general purpose registers

//reg eachvec;

// test vector input registers

reg [3:0] ain;

reg [3:0] bin;

reg cin;

// wires

wire cout;

wire [3:0] sum;

// assign statements (if any)

sub\_4bits i1 (

// port map - connection between master ports and signals/registers

.ain(ain),

.bin(bin),

.cin(cin),

.cout(cout),

.sum(sum)

);

initial

begin

// code that executes only once

// insert code here --> begin

ain=0;

bin=0;

cin=0;

#20

ain=6;

cin=1;

#30

bin=4;

cin=0;

#40

ain=11;

bin=2;

#50

bin=1;

cin=1;

#10

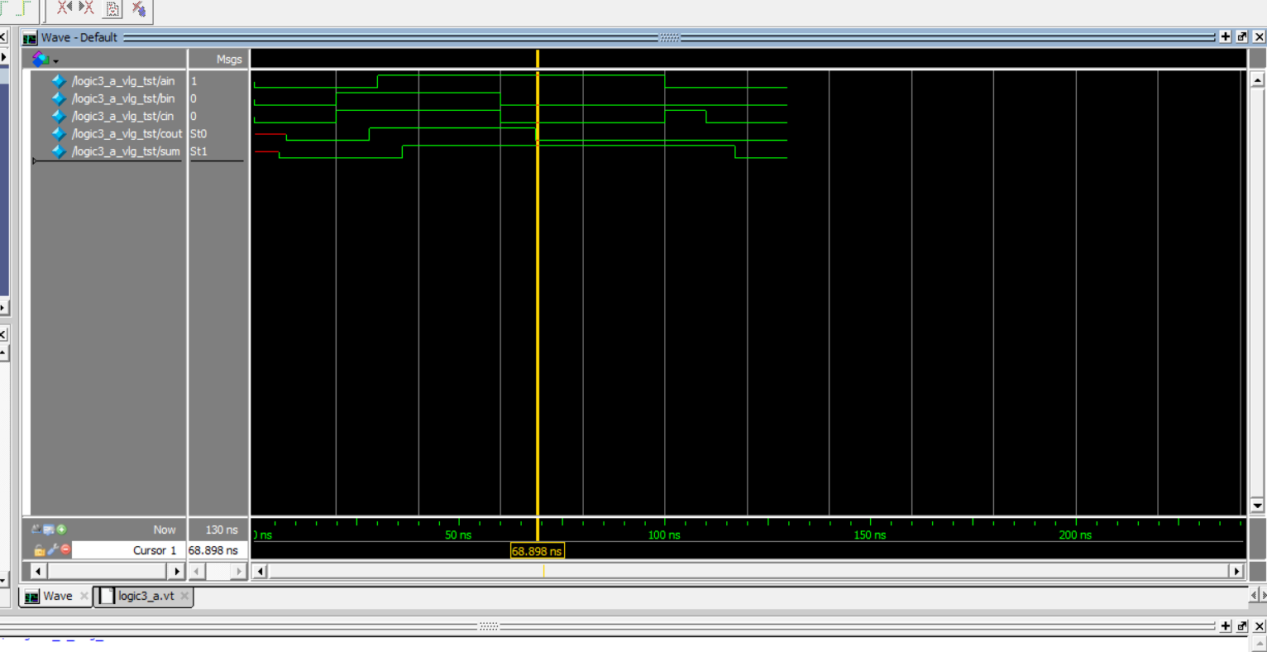
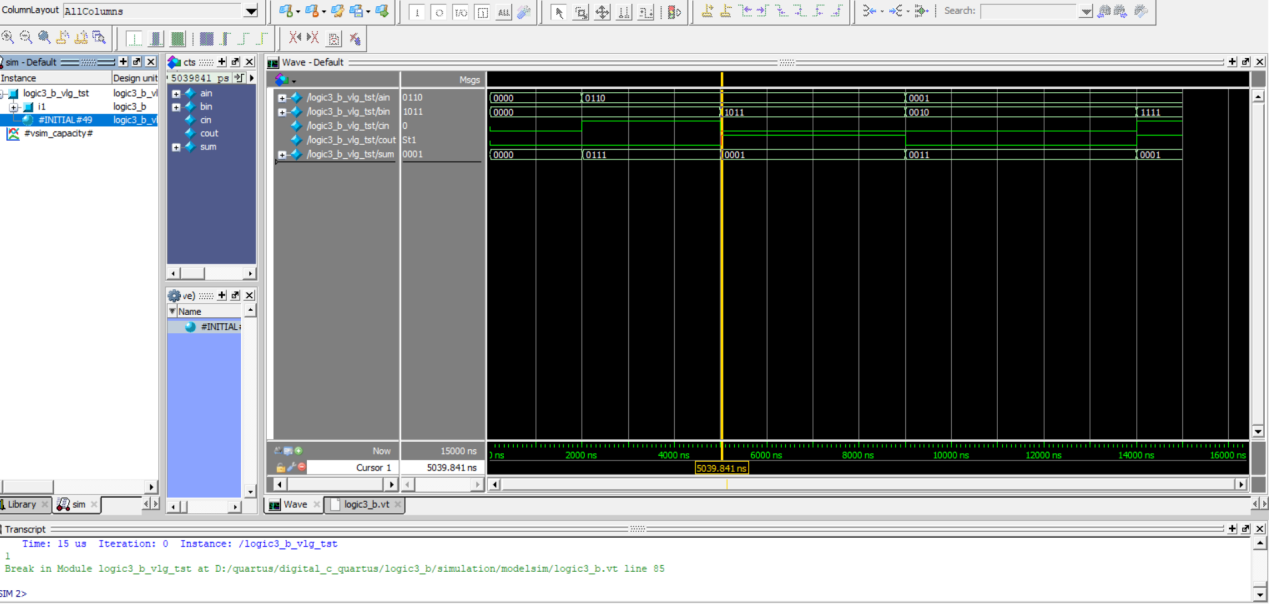
$finish;

// --> end

$display("Running testbench");

end

endmodule

5.Quartus仿真效果图（一位全加器、四位全加器、四位减法器）  
  
（1）全加器电路（截图）  
  
（2）四位全加器（截图）  
  
（3）四位减法器（截图）

